PCA2002

32 kHz watch circuit with programmable output period and pulse width

Rev. 04 — 7 September 2005 Product data sheet

1. General description

The PCA2002 is a CMOS integrated circuit for battery operated wrist watches with a 32 kHz quartz crystal as the timing element and a bipolar stepping motor. The crystal oscillator and the frequency divider are optimized for minimum current consumption. A timing accuracy of 1 ppm is achieved with a programmable, digital frequency adjustment.

The output period and the output pulse width can be programmed. It can be selected between a full output pulse or a chopped output pulse with a duty cycle of 75 %. In addition, a stretching pulse can be added to the primary driving pulse.

Pin RESET is used for stopping the motor, accurate time setting and for an accelerated testing of the watch.

2. Features

- 32 kHz quartz oscillator, amplitude regulated with excellent frequency stability and high immunity to leakage currents
- Electrically programmable time calibration with 1 ppm resolution (stored in OTP memory)
- The quartz crystal is the only external component required
- Very low current consumption: typically 90 nA
- Output pulses for bipolar stepping motors
- Five different programmable output periods (1 s to 30 s)
- Output pulse width programmable between 1 ms and 8 ms
- Full or chopped motor pulse and pulse stretching, selectable
- Stop function for accurate time setting and current saving during the shelf life
- Test mode for accelerated testing of the mechanical parts of the watch
- Test bits for type recognition (version B)

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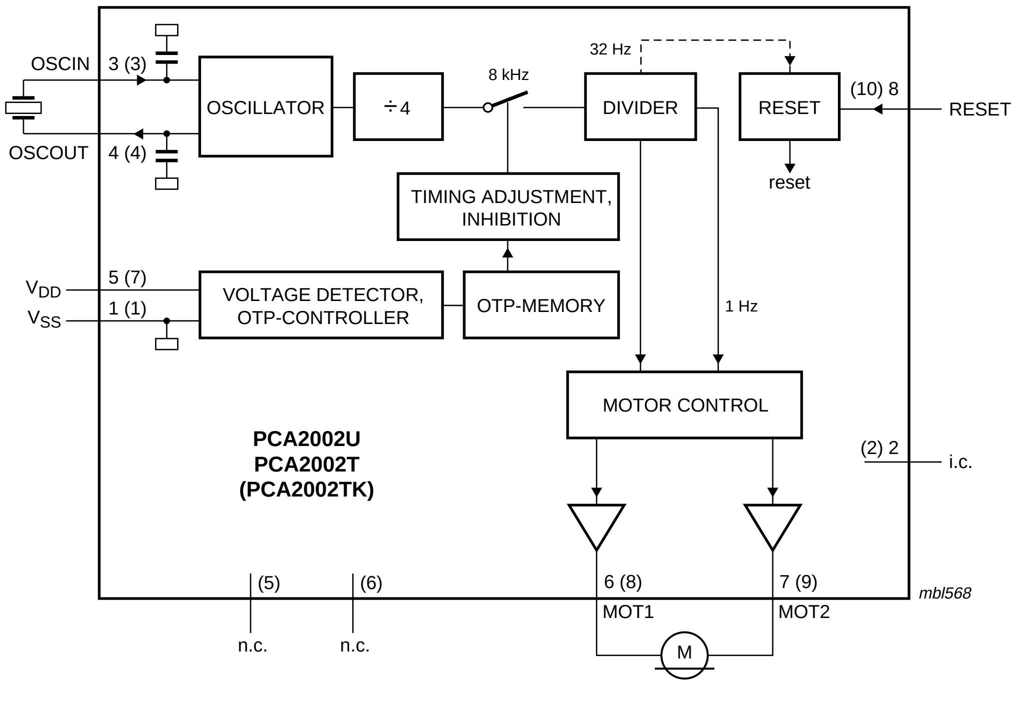
3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PCA2002U/AA	-	bare die; chip in tray	-
PCA2002U/AB	-	bare die; chip in tray	B
PCA2002U/10AA	-	bare die; chip on film frame carrier	-
PCA2002U/10AB	-	bare die; chip on film frame carrier	B
PCA2002T	PMFP8	plastic micro flat package; 8 leads (straight)	SOT144-1
PCA2002TK	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 × 3 × 0.85 mm	SOT650-1

4. Block diagram



The pin numbers given in parenthesis refer to the PCA2002TK

Fig 1. Block diagram

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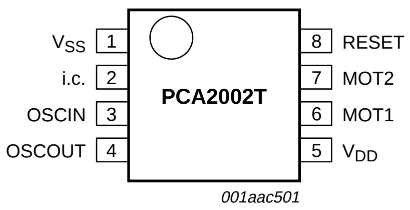
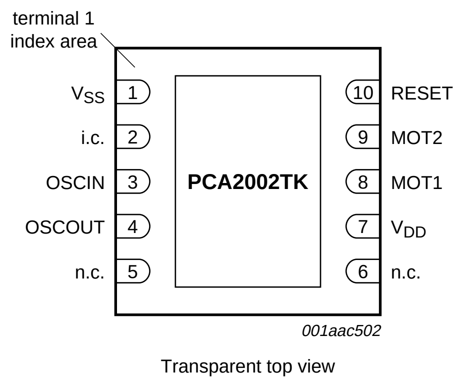
5. Pinning information

5.1 Pinning



a. PMFP8 (SOT144-1)



b. HVSON10 (SOT650-1)

Fig 2. Pin configuration

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
PCA2002T		
V_{SS}	1	ground supply
i.c.	2	internally connected
OSCIN	3	oscillator input
OSCOUT	4	oscillator output
V_{DD}	5	supply voltage
MOT1	6	motor 1 output
MOT2	7	motor 2 output
RESET	8	reset input
PCA2002TK		
V_{SS}	1	ground supply
i.c.	2	internally connected
OSCIN	3	oscillator input
OSCOUT	4	oscillator output
n.c.	5	not connected
n.c.	6	not connected
V_{DD}	7	supply voltage
MOT1	8	motor 1 output
MOT2	9	motor 2 output
RESET	10	reset input

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6. Functional description

6.1 Motor pulse

The motor driver delivers pulses with an alternating polarity. The output waveform across the motor terminals is illustrated in Figure 3. Between the motor pulses, both terminals are connected to V_{DD} which means that the motor is short-circuit.

The following parameters can be selected and are stored in a One Time Programmable (OTP) memory:

- Output periods of 1 s, 5 s, 10 s, 20 s and 30 s
- Pulse width (t_p) between 0.98 ms and 7.8 ms in steps of 0.98 ms
- Full or chopped (75 %) output pulse
- Pulse stretching: an enlargement pulse is added to the primary motor pulse. This enlargement pulse has a duty cycle of 25 % and a width which is twice the programmed motor pulse width.

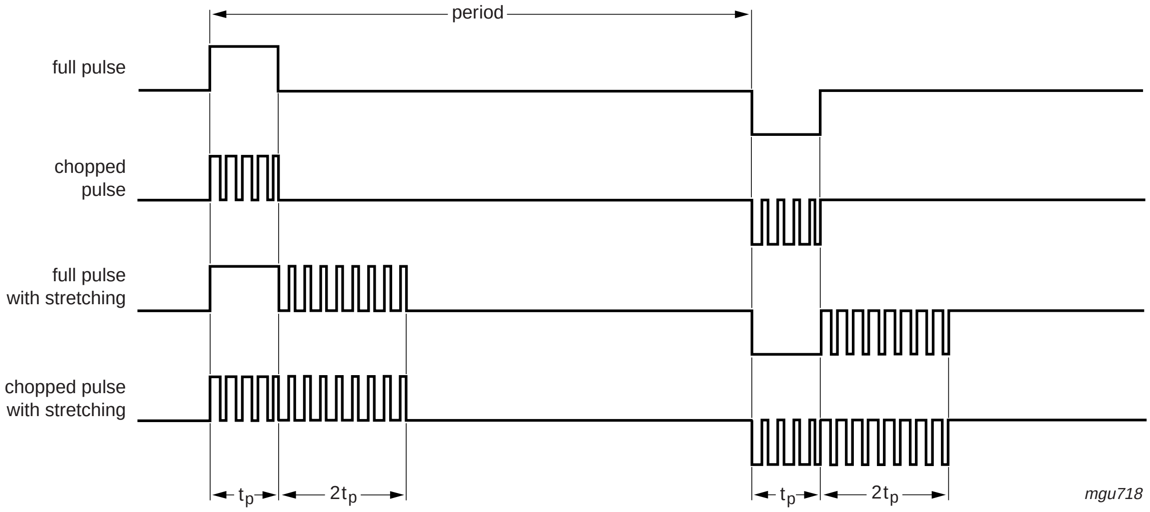

Fig 3. Motor output waveforms

6.2 Time calibration

The crystal oscillator has an integrated load capacitance of 5 pF, which is lower than the specified load capacitance of 8.2 pF for the quartz crystal.

It oscillates therefore, at a frequency which is typically 60 ppm higher than 32.768 Hz. This positive frequency offset is then compensated by removing, every minute or every two minutes, the appropriate number of 8192 Hz pulses (maximum 127 pulses) of the divider chain. The timing correction is given in Table 3.

After measuring the effective oscillator frequency, the number of correction pulses must be calculated and stored together with the calibration period in the OTP memory; see Section 6.6.

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The oscillator frequency can be measured at pin RESET, where a square wave with the frequency f_{osc} / 1024 is provided. It should be noted that this frequency shows a jitter every minute or every two minutes (depending on the programmed calibration period) which originates from the time calibration.

Details on how to measure the oscillator frequency and the programmed inhibition time are given in Section 6.6.

Table 3: Timing correction

Calibration period (min)	Correction per step (n = 1)		Correction per step (n = 127)	
	ppm	seconds per day	ppm	seconds per day
1	2.03	0.176	258	22.3
2	1.017	0.088	129	11.15

6.3 Reset

An output frequency of 32 Hz (f_{osc} / 1024) is provided at pin RESET. Connecting pin RESET to V_{DD} stops the motor drive and opens the motor switches.

After releasing pin RESET, the first motor pulse is generated exactly one period later with the opposite polarity to the last pulse before stopping. The debounce time for the reset function is between 31 ms and 62 ms.

Connecting pin RESET to V_{SS} activates the test mode. In this mode the motor output frequency is 32 Hz, which can be used to test the mechanical function of the watch.

6.4 Programming possibilities

The programming data is organized in an array of 8-bit words (see Table 4). A contains the time calibration, B the setting for the monitor pulses, C is not used and D contains the type recognition.

Table 4: Words and bits

Word	Bit							
	1	2	3	4	5	6	7	8
A	number of 8192 Hz pulses to be removed							calibration period
B	pulse width			output period			duty cycle	pulse stretching
C								
D	type				factory test bit			

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Table 5: Description of word A bits

Bit	Value	Description
Inhibit time		
1 to 7	-	the number of the 8192 Hz pulses to be removed (binary coded; MSB = A1 and LSB = A7)
Calibration period		
8	0	1 minute
	1	2 minutes

Table 6: Description of word B bits

Bit	Value	Description
Pulse width t_p (ms)		
1 to 3	000	0.98
	001	1.95
	010	2.9
	011	3.9
	100	4.9
	101	5.9
	110	6.8
	111	7.8
Output period (s)		
4 to 6	000	1
	001	5
	010	10
	011	20
	100	30
Duty cycle of motor pulse		
7	0	75 %
	1	100 %
Pulse stretching		
8	0	no pulse stretching
	1	a pulse width of $2t_p$ and a duty factor of 25 % are added

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6.5 Type recognition (version B only)

Byte D is read to determine which type of the PCA200X family is used in a particular application.

Table 7: Description of word D bits

Bit	Value	Description
Type recognition		
1 to 4	0000	PCA2002
	1000	PCA2000
	0100	PCA2001

6.6 Programming procedure

To ensure that the oscillator starts up correctly you must execute a reset sequence (see Figure 4).

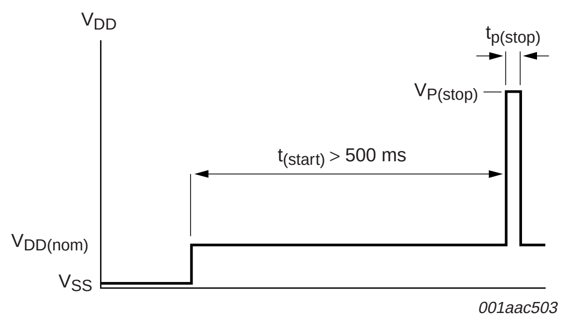

Fig 4. Supply voltage at start-up during production and testing

For a watch it is essential that the timing calibration can be made after the watch is fully assembled. In this situation, the supply pins are often the only terminals which are still accessible.

Writing to the OTP cells and performing the related functional checks is achieved in the PCA2002 by modulating the supply voltage. The necessary control circuit consists basically of a voltage level detector, an instruction state counter (which determines the function to be performed) and an 8-bit shift register which allows writing the OTP cells of an 8-bit word in one step and which acts as data pointer for checking the OTP content.

- State 1; measurement of the crystal oscillator frequency (divided by 1024)
- State 2; measurement of the inhibition time
- State 3; write/check word A
- State 4; write/check word B
- State 5; check word C
- State 6; check word D (type recognition)

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There are four different instruction states:

Each instruction state is switched on with a pulse to $V_{P(start)}$. After this large pulse, an initial waiting time of t_0 is required. The programming instructions are then entered by modulating the supply voltage with small pulses of an amplitude $V_{P(mod)}$ and pulse width t_{mod}. The first small pulse defines the start time, the following pulses perform three different functions, depending on the time delay (t_d) from the preceding pulse (see Figure 5):

- $t_d = t_1$ (0.7 ms); increments the instruction counter
- $t_d = t_2$ (1.7 ms); clocks the shift register with D = 0 at the input
- $t_d = t_3$ (2.7 ms); clocks the shift register with D = 1 at the input

The programming procedure requires a stable oscillator, which means that a waiting time, determined by the start-up time of the oscillator, is necessary after power-up of the circuit.

After the $V_{P(start)}$ pulse, the instruction counter is in State 1 and the data shift register is cleared. The instruction state ends with a second pulse to $V_{P(start)}$ or with the pulse to V_{store}. In any event the instruction states are terminated automatically 2 seconds after the last $V_{P(mod)}$ pulse.

6.6.1 Measurement of the oscillator frequency and the inhibition time

The output of the two measuring states can either be monitored directly at pin RESET or as a modulation of the supply current (a modulating resistor of 30 kΩ is connected between V_{DD} and V_{SS} when the signal at pin RESET is HIGH):

- State 1; crystal oscillator frequency divided by 1024; State 1 starts with a pulse to $V_{P(start)}$ and ends with a second pulse to $V_{P(stop)}$
- State 2; inhibition time (see Figure 5); a frequency with the period of (31.25 + n × 0.122) ms appears at pin RESET and as current modulation at the supply pin (see Figure 6)

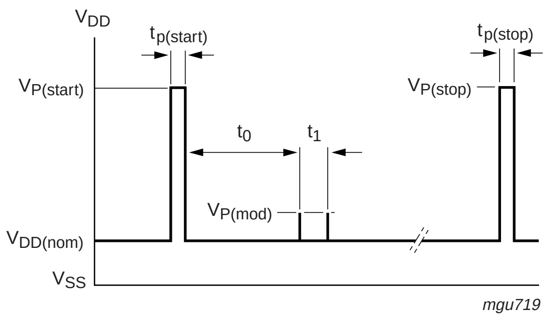

Fig 5. Supply voltage modulation for start and stop of instruction State 2

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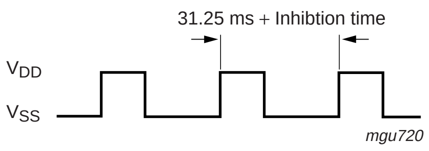

Fig 6. Output waveform at pin RESET for instruction State 2

6.6.2 Programming the memory cells

Applying the two-stage programming pulse (see Figure 7) transfers the stored data in the shift register to the OTP cells.

Perform the following to program a memory word:

1. Starting with a $V_{P(start)}$ pulse, wait for the time period t_0 then set the instruction counter to the word to be written ($t_d = t_1$).
2. Enter the data to be stored into the shift register ($t_d = t_2$ or t_3), LSB first (bit 8) and MSB last (bit 1).
3. Applying the two-stage programming pulse $V_{pre\text{-}store}$ followed by V_{store} stores the word. The delay between the last data bit and the pre-store pulse $V_{pre\text{-}store}$ is $t_d = t_4$. Store the word by raising the supply voltage to V_{store}; the delay between the last data bit and the store pulse is t_d.

The example shown in Figure 7 performs the following functions: start, setting the instruction counter to State 4 (word B), entering data word 1101 0001 into the shift register (sequence: LSB first and MSB last) and writing the OTP cells for word B.

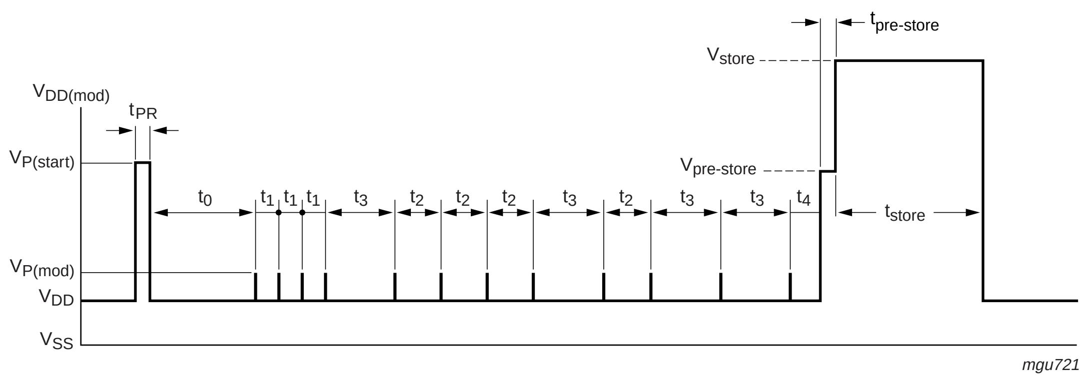

Fig 7. Supply voltage modulation for programming

6.6.3 Checking the memory content

The stored data of the OTP array can be checked bit-wise by measuring the supply current (see Figure 8). The array word is selected by the instruction state, the bit is addressed by the shift register. To read a word, the word is first selected ($t_d = t_1$) and a logic 1 is written into the first cell of the shift register ($t_d = t_3$).

This logic 1 is then shifted through the entire shift register ($t_d = t_2$, so that it points with each clock pulse to the next bit. If the addressed OTP cell contains a logic 1, a 30 kΩ resistor is connected between V_{DD} and V_{SS}; this increases the supply current accordingly.

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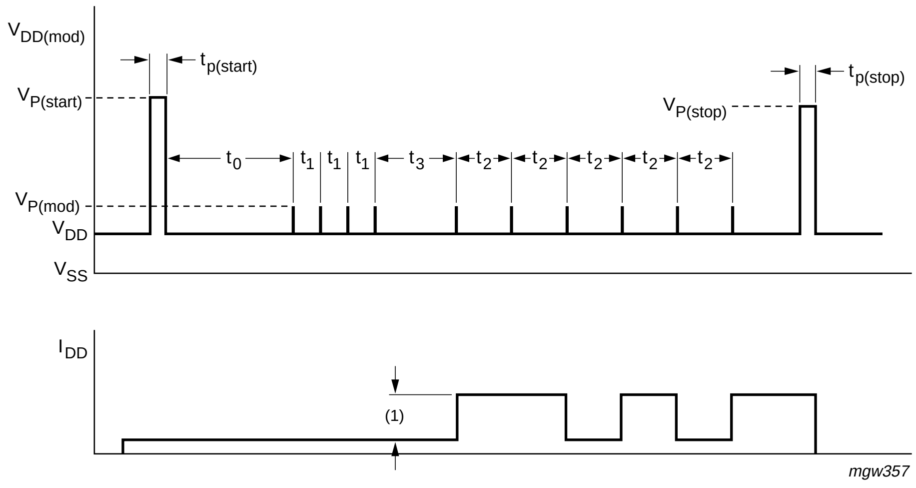

(1) $\Delta I_{DD} = \frac{V_{DD}}{30\ k\Omega}$

The corresponding supply current variation for B = 110101 (the sequence is MSB first and LSB last).

Fig 8. Supply voltage modulation for reading word B

6.7 Frequency tuning at assembled watch

Figure 9 shows the test set-up for frequency tuning the assembled watch.

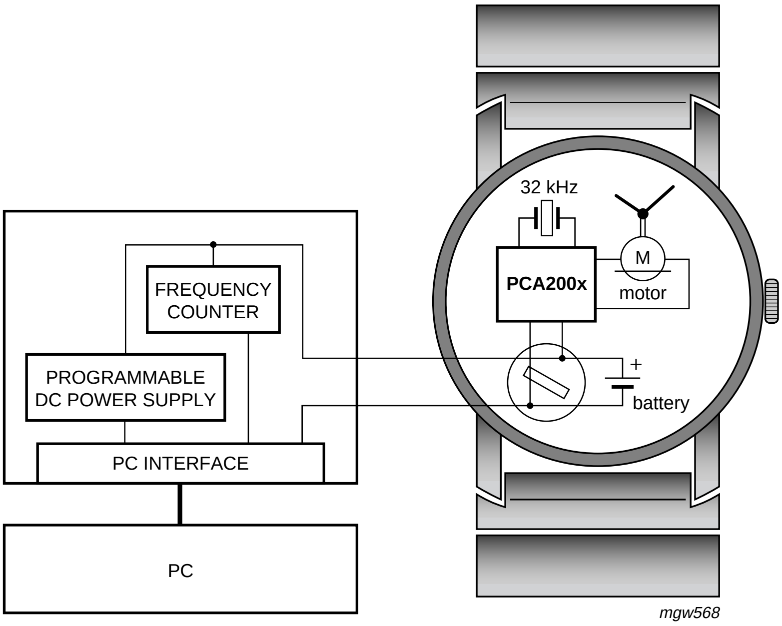

Fig 9. Frequency tuning the assembled watch

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7. Limiting values

Table 8: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	V_{SS} = 0 V	[1] [2]	–1.8	+7	V
V_I	all input voltages			V_{SS} – 0.5	V_{DD} + 0.5	V
$t_{o(sc)}$	output short-circuit duration			-	indefinite	s
T_{amb}	ambient temperature			–10	+60	°C
T_{stg}	storage temperature			–30	+100	°C

[1] When writing to the OTP cells, the supply voltage (V_{DD}) can be raised to a maximum of 12 V for a time period of 1 s.

[2] Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows which rapidly discharges the battery.

8. Characteristics

Table 9: Characteristics

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; quartz crystal: R_s = 40 kΩ, C_1 = 2 fF to 3 fF, C_L = 8.2 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage	normal operating mode; T_{amb} = –10 °C to +60 °C	1.1	1.55	3.6	V
ΔV_{DD}	supply voltage variation	ΔV/Δt = 1 V/µs	-	-	0.25	V
I_{DD}	supply current	between motor pulses	-	90	120	nA
		between motor pulses at V_{DD} = 3.5 V	-	120	180	nA
		T_{amb} = –10 °C to +60 °C	-	-	200	nA
		Stop mode; pin RESET connected to V_{DD}	-	100	135	nA
Motor output						
V_{sat}	saturation voltage Σ(P + N)	R_M = 2 kΩ; T_{amb} = –10 °C to +60 °C	-	150	200	mV
$Z_{o(sc)}$	short-circuit impedance	between motor pulses; I_{motor} < 1 mA	-	200	300	Ω
Oscillator						
V_{start}	starting voltage		1.1	-	-	V
g_m	transconductance	V_{OSCIN} ≤ 50 mV (p-p)	5	10	-	µS
t_{osc}	start-up time		-	0.3	0.9	s
Δf/f	frequency stability	ΔV_{DD} = 100 mV	-	0.05	0.2	ppm
C_{int}	integrated load capacitance		4.3	5.2	6.3	pF
R_{par}	parasitic resistance	allowed resistance between adjacent pins	20	-	-	MΩ

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Table 9: Characteristics *...continued*

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; quartz crystal: R_s = 40 kΩ, C_1 = 2 fF to 3 fF, C_L = 8.2 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset						
f_o	output frequency		-	32	-	Hz
ΔV_o	output voltage swing	R_L = 1 MΩ; C_L = 10 pF	1.4	-	-	V
t_r	rise time	R_L = 1 MΩ; C_L = 10 pF	-	1	-	µs
t_f	fall time	R_L = 1 MΩ; C_L = 10 pF	-	1	-	µs
$I_{i(av)}$	average input current	pin RESET connected to V_{DD} or V_{SS}	-	10	20	nA

9. OTP programming characteristics

Table 10: OTP programming characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage during programming procedure		1.5	-	3.0	V
$V_{P(start)}$	supply voltage for starting programming procedure		6.6	-	6.8	V
$V_{P(stop)}$	supply voltage for stopping programming procedure		6.2	-	6.4	V
$V_{P(mod)}$	supply voltage modulation for entering instructions		320	350	380	mV
$V_{pre\text{-}store}$	supply voltage for pre-store pulse		6.2	-	6.4	V
V_{store}	supply voltage for writing to the OTP cells		9.9	10.0	10.1	V
I_{store}	supply current for writing to the OTP cells		-	-	10	mA
$t_{p(start)}$	pulse width of start pulse		8	10	12	ms
$t_{p(stop)}$	pulse width of stop pulse		0.05	-	0.5	ms
t_{mod}	modulation pulse width		25	30	40	µs
$t_{pre\text{-}store}$	pulse width of pre-store pulse		0.05	-	0.5	ms
t_{store}	pulse width for writing to the OTP cells		95	100	110	ms
t_0	waiting time after start pulse		20	-	30	ms
t_1	pulse distance for incrementing the state counter		0.6	0.7	0.8	ms
t_2	pulse distance for clocking the data register with data = logic 0		1.6	1.7	1.8	ms
t_3	pulse distance for clocking the data register with data = logic 1		2.6	2.7	2.8	ms

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Table 10: OTP programming characteristics [1] *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_4	waiting time for writing to the OTP cells		0.1	0.2	0.3	ms
SR	slew rate for modulation of the supply voltage		0.5	-	5	V/µs
R_{read}	read-out resistor for supply current modulation		18	30	45	kΩ

[1] Program each word once only.

10. Bare die information

Table 11: Bonding pad locations

Symbol	Pad	Coordinates [1]	
		x	y
V_{SS} [2]	1	–480	+330
i.c. [3]	2	–480	+160
OSCIN	3	–480	–160
OSCOUT	4	–480	–330
V_{DD}	5	+480	–330
MOT1	6	+480	–160
MOT2	7	+480	+160
RESET	8	+480	+330

[1] All coordinates are referenced, in µm, to the center of the die (see Figure 10).

[2] The substrate (rear side of the chip) is connected to V_{SS}. Therefore, the die pad must be either floating or connected to V_{SS}.

[3] Pad i.c. is used for factory tests; in normal operation it should be left open-circuit, and it has an internal pull-down resistance to V_{SS}.

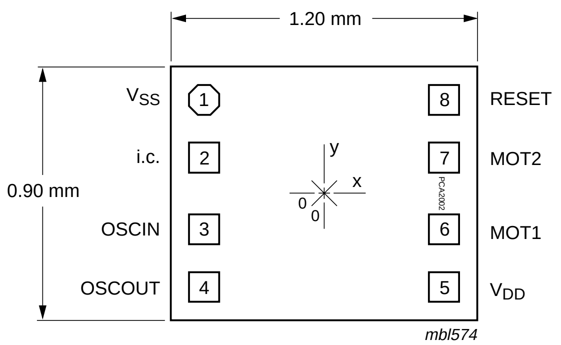

Fig 10. Bonding pad locations

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Table 12: Mechanical chip data [1]

Parameter	Value
Bonding pad	
metal	96 μm × 96 μm
opening	86 μm × 86 μm

[1] The substrate of the chip is connected to V_{SS}. The pad i.c. is used for factory test, in normal operation it should be left open-circuit. The pad i.c. has an internal pull-down resistor connected to V_{SS}.

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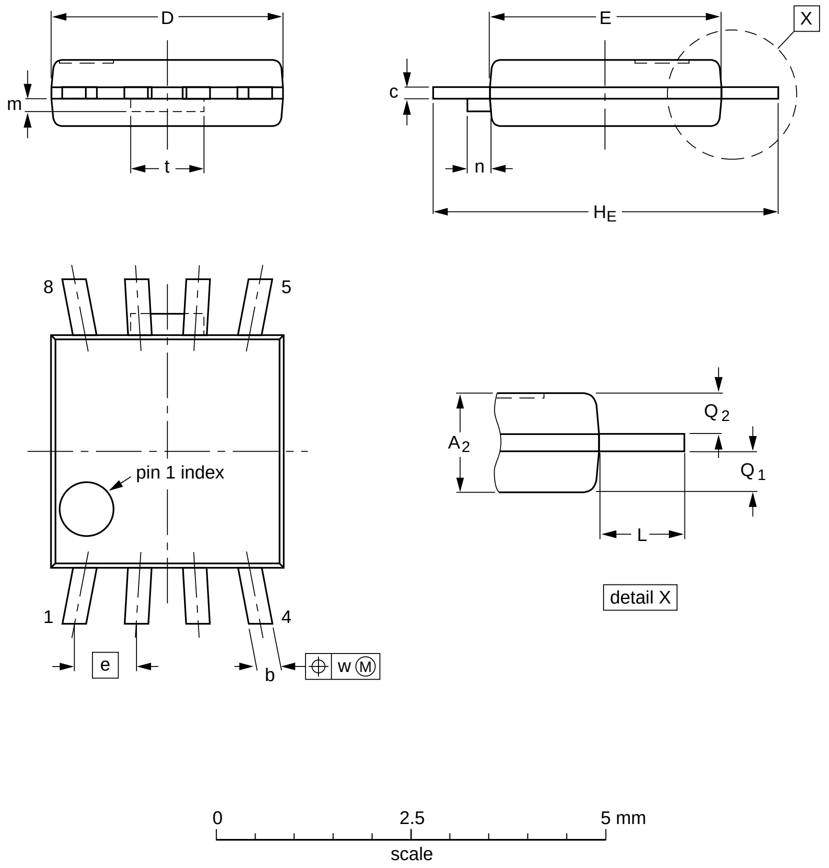
11. Package outline

PMFP8: plastic micro flat package; 8 leads (straight) **SOT144-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2	b	c	D (1)	E (1)	e	H_E	L	m max.	n max.	Q_1	Q_2	t	w
mm	0.9 0.7	0.40 0.25	0.19 0.12	3.1 2.9	3.1 2.9	0.8	4.6 4.4	0.75	0.26	0.3	0.4 0.3	0.4 0.3	0.95	0.1

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT144-1						~~95-01-24~~ 03-03-12

Fig 11. Package outline SOT144-1 (PMFP8)

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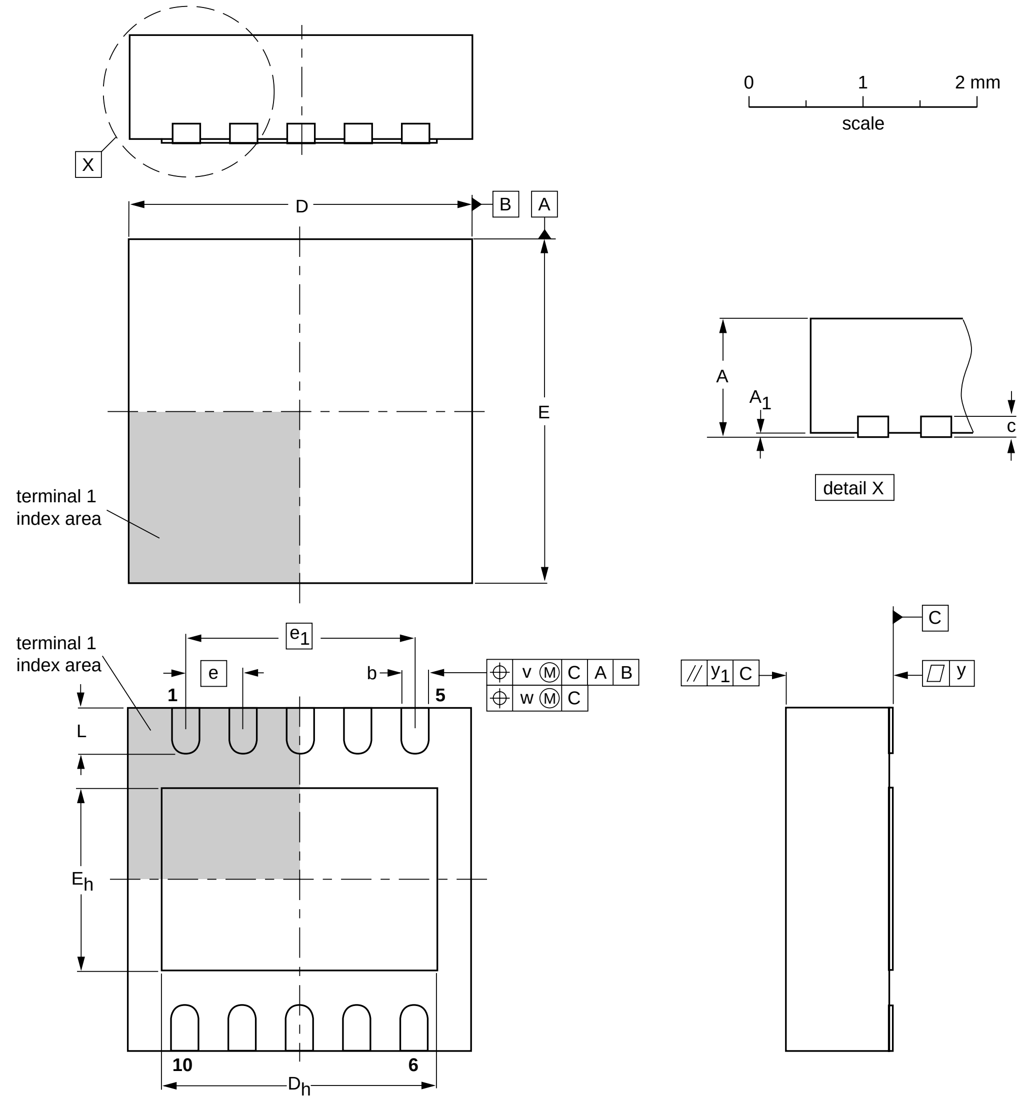
HVSON10: plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 x 3 x 0.85 mm **SOT650-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	2.55 2.15	3.1 2.9	1.75 1.45	0.5	2	0.55 0.30	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT650-1	- - -	MO-229	- - -			~~01-01-22~~ 02-02-08

Fig 12. Package outline SOT650-1 (HVSON10)

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12. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

13. Packing information

13.1 Tray information

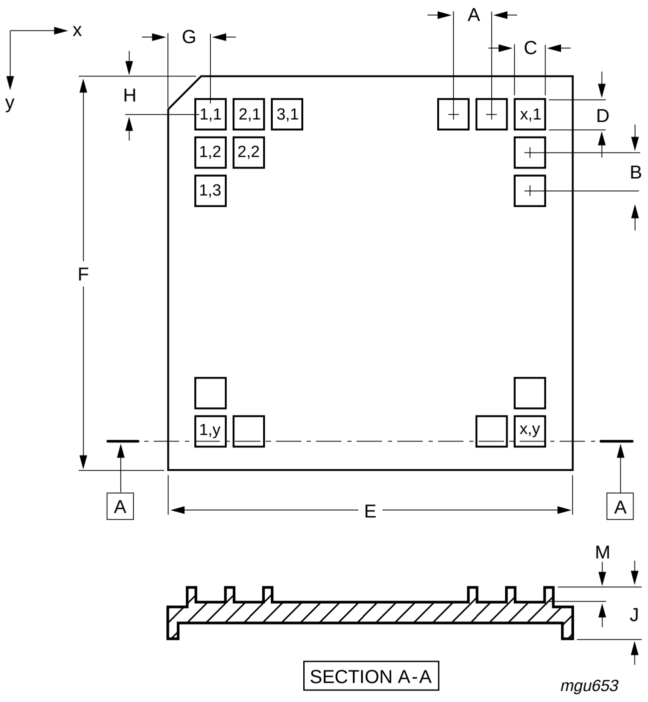

Fig 13. Tray details

Table 13: Tray dimensions

Dimension	Description	Value
A	pocket pitch; x direction	2.15 mm
B	pocket pitch; y direction	2.43 mm
C	pocket width; x direction	1.01 mm
D	pocket width; y direction	1.39 mm
E	tray width; x direction	50.67 mm
F	tray width; y direction	50.67 mm
G	distance from cut corner to pocket (1 and 1) center	4.86 mm
H	distance from cut corner to pocket (1 and 1) center	4.66 mm
J	tray thickness	3.94 mm

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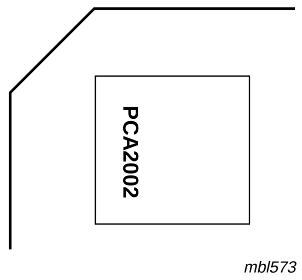
Table 13: Tray dimensions *…continued*

Dimension	Description	Value
M	pocket depth	0.61 mm
x	number of pockets in x direction	20
y	number of pockets in y direction	18



The orientation of the IC in a pocket is indicated by the position of the IC type name on the surface of the die, with respect to the cut corner on the upper left of the tray.

Fig 14. Tray alignment

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm

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   - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
   - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
   - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

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14.5 Package related soldering information

Table 14: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

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15. Revision history

Table 15: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCA2002_4	20050907	Product data sheet	-	9397 750 14617	PCA2002_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Version B added to data sheet – Section 2 "Features": Added version B feature – Section 3 "Ordering information": Added version B types – Section 6.4 "Programming possibilities": Added Word D description for version B – Section 6.6 "Programming procedure": Added word D remark for version B				
PCA2002_3	20040120	Product specification	-	9397 750 11671	PCA2002_2
PCA2002_2	20030204	Objective specification	-	9397 750 10986	PCA2002_1
PCA2002_1	20021025	Objective specification	-	9397 750 09659	-

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16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Date of release: 7 September 2005
Document number: 9397 750 14617

Published in The Netherlands